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Intel Legal Team

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Page 1 of 22

Urgent

Confidential

Date: September 17, 2004

To:
Examiner: H. Day
USPTO

Fax:
(703) 872-9306

Art Unit:
2123

From:
Paul E. Steiner

Fax:
703-633-3303

M/S:

Subject: Method and Apparatus for Modeling and Circuits with ...
Application No.: 09/531,910; Inventor: Sitaram Yadavalli, et al.
Filed: 3/20/00 Docket No. P7896

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Fax Cover Sheet (1 page)
Transmittal Form (1 page)
Fee Transmittal (1 page in duplicate)
Appeal Brief (18 pages)

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PTO/SB/21 (08-03)


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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/531,910	
	Filing Date	March 20, 2000	
	First Named Inventor	Sitaram Yadavalli	
	Art Unit	2123	
	Examiner Name	H. Day	
Total Number of Pages in This Submission	22	Attorney Docket Number	P7896

ENCLOSURES (Check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input checked="" type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance communication to Technology Center (TC) <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Fax Cover Sheet
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Paul E. Steiner, Reg. No. 41,326 Intel Americas, Inc.
Signature	
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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$ 330.00)

Complete if Known

Application Number	09/531,910
Filing Date	March 20, 2000
First Named Inventor	Sitaram Yadavalli
Examiner Name	H. Day
Art Unit	2123
Attorney Docket No.	P7896

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None
☒ Deposit Account:
 Deposit Account Number: 50-0221
 Deposit Account Name: Intel Corporation

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 770	2001 385	Utility filing fee	
1002 340	2002 170	Design filing fee	
1003 530	2003 265	Plant filing fee	
1004 770	2004 385	Reissue filing fee	
1005 160	2005 80	Provisional filing fee	

SUBTOTAL (1) (\$)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims: 20** = ☐ X ☐ = ☐
 Independent Claims: 3** = ☐ X ☐ = ☐
 Multiple Dependent: ☐ = ☐

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1202 18	2202 9	Claims in excess of 20	
1201 86	2201 43	Independent claims in excess of 3	
1203 280	2203 145	Multiple dependent claim, if not paid	
1204 86	2204 43	** Reissue independent claims over original patent	
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) (\$)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	2053 130	Non-English specification	
1812 2,520	2812 2,520	For filing a request for <i>ex parte</i> reexamination	
1804 920*	2804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	2805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 420	2252 210	Extension for reply within second month	
1253 950	2253 475	Extension for reply within third month	
1254 1,480	2254 740	Extension for reply within fourth month	
1255 2,010	2255 1,005	Extension for reply within fifth month	
1401 330	2401 165	Notice of Appeal	
1402 330	2402 165	Filing a brief in support of an appeal	330.00
1403 290	2403 145	Request for oral hearing	
1451 1,510	2451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,330	2453 665	Petition to revive - unintentional	
1501 1,330	2501 665	Utility issue fee (or reissue)	
1502 480	2502 240	Design issue fee	
1503 640	2503 320	Plant issue fee	
1460 130	2460 130	Petitions to the Commissioner	
1807 50	2807 50	Processing fee under 37 CFR 1.17(q)	
1806 180	2806 180	Submission of Information Disclosure Stmt	
8021 40	28021 40	Recording each patent assignment per property (times number of properties)	
1809 770	2809 385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 770	2810 385	For each additional invention to be examined (37 CFR 1.129(b))	
1801 770	2801 385	Request for Continued Examination (RCE)	
1802 900	2802 900	Request for expedited examination of a design application	

Other fee (specify):

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 330.00)

SUBMITTED BY

Name (Print/Type) Paul E. Steiner

Registration No. 41,326

(Complete if applicable)

Telephone 703-633-6830

Signature

Date

9/17/04

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DUPLICATE

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**FEE TRANSMITTAL
for FY 2004**

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT (\$)** 330.00**Complete if Known**

Application Number 09/531,910

Filing Date March 20, 2000

First Named Inventor Sitaram Yadavalli

Examiner Name H. Day

Art Unit 2123

Attorney Docket No. P7896

METHOD OF PAYMENT (check all that apply)☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☒ Deposit Account:Deposit Account Number
Deposit Account Name

50-0221

Intel Corporation

The Director is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments☒ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
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1002 340	2002 170	Design filing fee	
1003 530	2003 265	Plant filing fee	
1004 770	2004 386	Reissue filing fee	
1005 180	2005 80	Provisional filing fee	
SUBTOTAL (1) (\$)			

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent Claims	-20** =	X	
Multiple Dependent	-3** =	X	

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
1202 16	2202 9	Claims in excess of 20
1201 86	2201 43	Independent claims in excess of 3
1203 290	2203 145	Multiple dependent claim, if not paid
1204 86	2204 43	** Reissue independent claims over original patent
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SUBTOTAL (2) (\$)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity - Small Entity

Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
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1802 900	1802 900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$) 330.00**SUBMITTED BY**

Name (Print/Type) Paul E. Steiner

Registration No. 41,326
(Attorney/Agent)

Telephone 703-633-6830

Signature

Date

9/17/04

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**RECEIVED
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SEP 17 2004**

In re patent application of:

Sitaram YADAVALLI, et al.

Serial No.: 09/531,910

Group Art Unit: 2123

Filed: March 20, 2000

Examiner: H. Day

FOR: METHOD AND APPARATUS FOR MODELING AND CIRCUITS
WITH ASYNCHRONOUS BEHAVIOR**APPEAL BRIEF**Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits this appeal brief, thus perfecting the notice of appeal filed on July 19, 2004.

The required headings and subject matter follow.

(i) *Real party in interest.*

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) *Related appeals and interferences.*

There are no known related appeals and / or interferences.

(iii) *Status of claims.*

Claims 22-39 are pending in the case and stand rejected. The rejections of claims 22-39 are being appealed.

P7896

Serial No.: 10/054,083

(iv) Status of amendments.

After the final rejection, an amendment was filed on April 20, 2004. The advisory action mailed June 28, 2004 indicates that the amendment is entered. The attached Claims appendix reflects the current status of amendments.

(v) Summary of claimed subject matter.

The independent claims 22, 27, and 34 are respectively directed to a method, a system, and a set of instructions, including generating a netlist model for a circuit (page 9, lines 12-13, Fig. 6, block 62); providing a virtual delay element in the netlist model (page 9, lines 15-16, Fig. 6, block 64); providing a virtual clock signal to the virtual delay element (page 9, lines 18-19, amended Fig. 6, block 66) to influence a desired race resolution for the circuit (page 9, line 18, see also page 6, lines 28-29 and page 8, lines 14-16); and generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element (page 9, lines 13-15, amended Fig. 6, block 68). In claim 27, the system further includes a processor (page 6, lines 9-13, Fig. 2, CPU 18) and a memory (page 6, lines 9-13, Fig. 2, memory 20).

(vi) Grounds of rejection to be reviewed on appeal.

I. Claims 22-39 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

II. Claims 23, 29, and 35 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

III. Claims 22-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,798,645 (Zeiner), in view of U.S. Patent No. 5,649,176 (Selvidge) and further in view of U.S. Patent No. 5,938,753 (Dargelas).

Serial No.: 10/054,083

(vii) *Argument.*

- I. The rejection of claims 22-39 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention, is in error and should be reversed.

Claims 22, 28, and 34

With respect to claims 22, 28, and 34, the Examiner objected to the claim language relating to identifying a race condition in a circuit. The advisory action mailed June 28, 2004 fails to state the status of this rejection. Accordingly, applicants find it necessary to re-address this rejection in this appeal brief.

Applicants disagree with the Examiner's position, but have deleted this language from these claims, rendering this rejection moot. Applicants note that the deletion of the respective phrases is a broadening amendment, and applicants do not surrender any claim scope or equivalents by way of the present amendments.

Because the language which was objected to has been deleted, the rejection of claims 22, 28, and 34 should be reversed.

Claims 25, 31, and 37

With respect to claims 25, 31, and 37, the Examiner asserts that the recitation "with a physical characteristic of the circuit" does not appear to have support in the original disclosure. The advisory action mailed June 28, 2004 fails to clarify the status of this rejection. The advisory action does state:

2. Arguments regarding rejections are not persuasive. For example, "physical characteristics" (e.g., temperature or impurity) and "delay characteristics" are not identical. Please see Office Action mailed January 20, 2004, per rejections.

Serial No.: 10/054,083

Applicants are unable to identify any portion of Applicants' response to which the Examiner's comments might be directed. Accordingly, applicants find it necessary to re-address this rejection in this appeal brief.

The rejection is not understood. The Examiner objects to the phrase "with a physical characteristic of the circuit" even though the Examiner has identified corresponding support in the specification that explicitly states "characteristics of the physical circuit" at page 8, lines 10-12. Applicants submit that this portion alone provides ample support for the claim language. Literal word for word support for the claim language is not required so long as one skilled in the art would appreciate that the claim language is supported by the description and the drawings. In any event, reference is made throughout the specification to various physical characteristics of the circuit including the non-limiting examples of "exact delay characteristics" (page 8, lines 10-12), "die and chip architecture constraints" (page 2, line 8), operational speed of gates (page 2, line 9), "the lengths of conductive paths between circuit elements" (page 2, lines 9-10), and "specific routing directions and positions of each element" (page 2, line 10). Those skilled in the art would appreciate that other physical characteristics of the circuit may also be covered by the claim language.

Applicants note that the rejection mentions "undue experiment," which is irrelevant to the written description rejection at hand. In any event, MPEP § 2163(II)(A)(2) correctly states that "[i]nformation which is well known in the art need not be described in detail in the specification." The Examiner has asserted in connection with the § 103 rejection of claim 25 that Selvidge describes a virtual clock signal is specified in accordance with a physical characteristic of the circuit. Although applicants disagree with this assertion, assuming for the sake of argument that the Examiner is correct, then by the Examiner's own admission one skilled in the art would know how to specify the virtual clock signal in accordance with a physical characteristic of a circuit.

Applicants submit that the claim language is well supported in the specification as filed, and further that one skilled in the art, having the benefit of the present specification, would

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understand how to specify the virtual clock signal in accordance with a physical characteristic of the circuit. Accordingly, the rejection of claims 25, 31, and 37 should be reversed.

Claims 27, 33, and 39

With respect to claims 27, 33, and 39, the Examiner asserts that the recitation "the delay characteristic corresponds to a length of conductive paths between circuit elements" does not appear to have support in the original disclosure. The advisory action mailed June 28, 2004 fails to state the status of this rejection. Accordingly, applicants find it necessary to re-address this rejection in this appeal brief.

Support for the claim language is explicitly provided on page 2, lines 9-10, which describes how a delay in a circuit may be caused by "the lengths of conductive paths between circuit elements." Support is also found in the paragraph on page 2, lines 11-20, which describes how a delay may be caused "if second conductive path 12 is of much greater length than first conductive path 8" (see page 2, lines 11-12). Finally, support is provided by page 6, line 28 through page 7, line 8, which describes how data traveling on like numbered second conductive path 12 takes a long time relative to data traveling on like numbered first conductive path 8.

The Examiner has asserted in connection with the § 103 rejection of claim 27 that Selvidge describes a delay physical characteristic which corresponds to a length of conductive paths between circuit elements. Although applicants disagree with this assertion, assuming for the sake of argument that the Examiner is correct, then by the Examiner's own admission it is "well known" to specify a delay physical characteristic which corresponds to a length of conductive paths between circuit elements.

Applicants submit that the present disclosure fully supports the claims, and further that one of ordinary skill in the art, having the benefit of the present specification, would understand how the delay characteristic may correspond to a length of conductive paths between circuit elements. Accordingly, the rejection of claims 27, 33, and 39 should be reversed.

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Claims 23, 24, 26, 29, 30, 32, 35, 36, and 38:

The remaining claims are rejected only because of their dependency on a rejected base claims. Accordingly, the rejection of these claims should be reversed along with the reversal of their respective base claims.

- II. The rejection of claims 23, 29, and 35 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention, is in error and should be reversed.

Claims 23, 29, and 35:

With respect to claims 23, 29, and 35, the Examiner asserts that the claim language "selectively providing a virtual delay element for respective sequential elements in the circuit" is not enabled. However, the Examiner has not completed the analysis required to establish a prima facie case of lack of enablement. For example, the Examiner asserts that undue experimentation would be required to practice the claim recitations, but fails to provide analysis of any of the undue experimentation factors. The relevant factors are set forth in MPEP § 2164.01(a), which further states "[t]he examiner's analysis must consider all the evidence related to each of these factors, and any conclusion of nonenablement must be based on the evidence as a whole." (Emphasis added). If the rejection is maintained, applicants respectfully request that the Examiner perform the complete analysis as required MPEP § 2164 and articulate both the analysis and the results in the Examiner's answer, so that a full and fair reply may be made.

In any event, the claim recitations are well described in the specification, fully supported and enabled. At page 8, lines 14-19, the present specification describes:

According to an embodiment of the present invention, race resolution at every sequential element can be individually controlled by the introduction of virtual delay elements controlled by corresponding virtual clocks in the appropriate path. Therefore, each sequential element can have its own race

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resolution mechanism. For example in sequential circuit 29, if control over the arrival time of data1 is required by ATPG, then a virtual delay element 38 may be added along the path of the data1 input to flip-flop 30.

For example, the foregoing describes that race resolution may be determined on an individual basis for each sequential element. For example, the virtual delay element 38 may be provided if the ATPG requires control over the arrival time of data1. For example, in various of the figures, some sequential elements have associated virtual delay elements while others do not. In fact, throughout the specification and drawings, the concept of adding virtual delay elements where such control is needed is described.

Applicants again note that the Examiner's position with respect to enablement is inconsistent with the Examiner's position in the § 103 rejection that the claim language is taught by the prior art. MPEP § 2164.01 correctly states that "[a] patent need not teach, and preferably omits, what is well known in the art." The Examiner has asserted in connection with the § 103 rejection of claim 23 that Selvidge describes providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential element. Although applicants disagree with this assertion, assuming for the sake of argument that the Examiner is correct, then by the Examiner's own admission one skilled in the art would know how to selectively provide a virtual delay element for respective sequential elements in the circuit.

Applicants submit that the present disclosure more than adequately enables one of ordinary skill in the art to practice claims 23, 29, and 35. Accordingly, the rejection of claims 23, 29, and 35 should be reversed.

Serial No.: 10/054,083

III. The rejection of claims 22-39 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,798,645 (Zeiner), in view of U.S. Patent No. 5,649,176 (Selvidge) and further in view of U.S. Patent No. 5,938,753 (Dargelas), is in error and should be reversed.

Claims 22, 24, 28, 30, 34 and 36:

Each of the independent claims 22, 28, and 34 recite features relating to:

- generating a netlist model for a circuit;
- providing a virtual delay element in the netlist model;
- providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and
- generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.

By way of background, the invention as presently claimed is directed to the problem of test pattern generation for a circuit which may have a race condition which requires race resolution in order to generate a valid test pattern. None of the cited references are directed to this problem. In fact, Dargelas fails to even mention race resolution, Selvidge mentions race conditions only tangentially in terms of hold time violations, and Zeiner addresses the problems of race conditions in a physical device with physical delay element.

Applicants first note that is highly unlikely that one of ordinary skill in the art would be motivated to find and make the myriad of modifications required by the combination of the three cited references, absent the benefit of the present specification. Of the foregoing claim recitations, the Examiner's primary reference, Zeiner, is relied upon for only a single aspect of the claims, namely generating a netlist model. The Examiner admits that the primary reference fails to teach or suggest the recited providing a virtual delay element, providing a virtual clock, and generating a test pattern, and relies on the two other references to piece together the rejection. The Examiner fails to provide sufficient explanation as to why one skilled in the art would be motivated to modify Zeiner, which admittedly lacks three of the four claim recitations,

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from a hardware emulation system, to a test pattern generation system utilizing virtual elements. Clearly, the proposed modification relies heavily on impermissibly utilizing the claim as a blueprint for piecing together the various modifications.

Moreover, any motivation to combine the references fails for at least the following reasons. Zeiner has already solved the problem of internal race conditions by the utilization of physical, programmable delay devices. The Examiner has not provided any explanation as to why anyone would be motivated to replace the physical, programmable delay devices in Zeiner with the virtual, clocked elements of Selvidge. It is certainly not clear that such a substitution would result in an operative device.

The Examiner suggests that the virtual element and virtual clock of Selvidge is simply the detailed implementation of the programmable delay unit in Zeiner. However, this is incorrect. A programmable delay unit has entirely different operating characteristic than a clocked delay element. Moreover, making the proposed modification would change the fundamental operating principle of Zeiner. Namely, Zeiner provides an actual hardware emulation unit containing physical devices, not virtual devices.

As noted above, the claims recite providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit. The Examiner fails to give full consideration to each element of this claim recitation. The office action cites "Selvidge, virtual clock VClk I Fig. 16B: and column 18, lines 58-63" against this claim recitation. However, the Examiner's analysis completely ignores the claim language of "to influence a desired race resolution for the circuit." The cited portion of Selvidge follows:

An example is shown in Fig. 16A, this implicit state can be transformed into an explicit state element which is clocked by the virtual clock VClk by simply choosing a wire 1601 in the loop and inserting a flip-flop 1602 which is clocked by the virtual clock VClk as shown in Fig. 16B.

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From the foregoing, Selvidge discloses providing a virtual clock to a flip-flop to transform an implicit state into an explicit state. However, the cited portion is silent with respect to influencing a desired race resolution for the circuit. Accordingly, the Examiner has failed to establish a prima facie case of obviousness.

Finally, admitting that Zeiner (and Selvidge) fails to teach or suggest the recited generating a test pattern, the Examiner relies on yet another reference, Dargelas for this further missing teaching. Specifically, the office action asserts that the abstract of Dargelas discloses generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element. Again, the Examiner has failed to give full consideration to each claim element. While Dargelas discloses determining test patterns, the cited portion is silent with respect to other aspects of the claim recitation. Applicants have thoroughly studied the abstract of Dargelas and can find no mention of virtual delay elements or virtual clocks. Accordingly, the Examiner has failed to establish a prima facie case of obviousness.

In any event, the Examiner has not provided an explanation of why one of ordinary skill in the art would be motivated to modify the hardware emulation system described by Zeiner to become or incorporate an automatic test pattern generator. The office action simply fails to address the claim as a whole and impermissibly uses the claim as a blueprint to pick and choose selected pieces of the prior art.

Because there is no motivation to modify the teachings of Zeiner with the teachings of Selvidge, and with the further teachings of Dargelas, claims 22, 28, and 34 are patentable over the cited combination of references. Further, because the Examiner fails to establish a prima facie case of obviousness, claims 22, 28, and 34 are patentable over the cited combination of references. Their respective dependent claims, including claims 24, 30, and 36, are likewise patentable.

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Claims 23, 29, and 35:

With respect to claims 23, 29, and 35, the claims recite selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

The Examiner fails to give full consideration to each element of this claim recitation. The office action cites the same portion of Selvidge, namely column 18, lines 58-63. However, this analysis completely ignores the claim language of "in accordance with respective race resolution requirements of the respective sequential elements." The cited portion of Selvidge follows:

An example is shown in Fig. 16A, this implicit state can be transformed into an explicit state element which is clocked by the virtual clock VClk by simply choosing a wire 1601 in the loop and inserting a flip-flop 1602 which is clocked by the virtual clock VClk as shown in Fig. 16B.

From the foregoing, Selvidge discloses providing a virtual clock to a flip-flop to transform an implicit state into an explicit state. However, the cited portion is silent with respect to race resolution requirements. Accordingly, the Examiner has failed to establish a prima facie case of obviousness and claims 23, 29, and 35 are separately patentable for at least that reason.

Claims 25, 31, and 37:

With respect to claims 25, 31, and 37, the claims recite that the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit. The portion of Selvidge relied upon by the Examiner, namely col. 18, lines 65-67, describes a logical characteristic of the circuit, not a physical characteristic. For the Examiner's convenience the cited portion is reproduced below:

Additional virtual clock cycles are required for the values in the loop to settle into their final states.

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The cited portion is silent with respect to any physical characteristic of the circuit. Accordingly, the office action fails to establish a prima facie case and claims 25, 31, and 37 are separately patentable for at least that reason.

Claims 26, 32, and 38:

With respect to claims 26, 32, and 38, these claims depend from claims 25, 31, and 37, respectively and recite that the physical characteristic comprises a delay characteristic. Read together with their base claims, the claims recite that the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit, wherein the physical characteristic comprises a delay characteristic.

The delay "period" described in col. 19, lines 1-14 of Selvidge does appear to correspond to any physical characteristic of the circuit, but rather only to a number of simulation cycles required for logical states to settle. In any event, the VClk described in Selvidge is not specified in accordance with the identified delay "period." Accordingly, the office action fails to establish a prima facie case and claims 26, 32, and 38 are separately patentable for at least that reason.

Claims 27, 33, and 39:

With respect to claims 27, 33, and 39, the claims recite that the delay characteristic corresponds to a length of conductive paths between circuit elements.

The nested loops described in col. 19, lines 1-14 of Selvidge relate only to the logical structure and not the physical structure. The cited portion is devoid of any description related to lengths of conductive paths. Accordingly, the office action fails to establish a prima facie case and claims 27, 33, and 39 are separately patentable for at least that reason.

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CONCLUSION

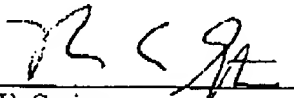
In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

September 17, 2004

Date

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office at (703) 872-9306 on September 17, 2004.

Paul E. Steiner 

Date: September 17, 2004

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(viii) Claims appendix.

- 1-21. (canceled).
22. A method, comprising:
generating a netlist model for a circuit;
providing a virtual delay element in the netlist model;
providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and
generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.
23. The method as recited in claim 22, further comprising:
selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.
24. The method of claim 22, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.
25. The method of claim 24, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.
26. The method of claim 25, wherein the physical characteristic comprises a delay characteristic.
27. The method of claim 26, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

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28. A system, comprising:
a processor; and
a memory coupled to the processor, the memory storing a program adapted to:
generate a netlist model for a circuit;
provide a virtual delay element in the netlist model;
provide a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and
generate a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.
29. The system as recited in claim 28, wherein the program is further adapted to selectively provide a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.
30. The system of claim 28, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.
31. The system of claim 30, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.
32. The system of claim 31, wherein the physical characteristic comprises a delay characteristic.
33. The system of claim 32, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

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34. A set of instructions residing in a storage medium, the set of instructions being capable of execution by a processor to implement a method, the method comprising:
- generating a netlist model for a circuit;
 - providing a virtual delay element in the netlist model;
 - providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and
 - generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.
35. The set of instructions as recited in claim 34, wherein the method further comprises:
- selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.
36. The set of instructions of claim 34, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.
37. The set of instructions of claim 36, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.
38. The set of instructions of claim 37, wherein the physical characteristic comprises a delay characteristic.
39. The set of instructions of claim 38, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

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(ix) *Evidence appendix.*

None.

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(x) *Related proceedings appendix.*

None.